

The listing of claims will replace all prior versions, and listings, of claims in the application:

**Listing of Claims:**

1. (Currently Amended) A clocked inverter comprising:  
a first transistor and a second transistor connected in series,  
a third transistor and a fourth transistor connected in series, and  
a fifth transistor and a sixth transistor connected in series, wherein:  
gates of the third transistor and the fourth transistor are connected to each other,  
drains of the third transistor and the fourth transistor are each connected to a gate of the first transistor,  
sources of the first transistor and the fourth transistor are each electrically connected to a first power source,  
sources of the second transistor and the sixth transistor are electrically connected to a second power source,  
gates of the fifth transistor and the sixth transistor are connected to each other,  
drains of the fifth transistor and the sixth transistor are each connected to a gate of the second transistor,  
a first signal is inputted to a source of the third transistor,  
a second signal is inputted to a source of the fifth transistor,  
the first signal is different from the second signal,  
an amplitude of [[a]] ~~the first signal inputted to a source of the third transistor~~ is smaller than a potential difference between the first power source and the second power source, and  
an amplitude of [[a]] ~~the second signal inputted to a source of the fifth transistor~~ is smaller than the potential difference between the first power source and the second power source.

2. (Previously Presented) A clocked inverter according to claim 1, wherein:  
the first power source is a high potential power source;  
the second power source is a low potential power source;  
the first transistor, the fourth transistor, and the fifth transistor are each a P-type transistor; and  
the second transistor, the third transistor, and the sixth transistor are each an N-type transistor.
3. (Previously Presented) A clocked inverter according to claim 1, wherein:  
the first power source is a low potential power source;  
the second power source is a high potential power source;  
the first transistor, the fourth transistor, and the fifth transistor are each an N-type transistor; and  
the second transistor, the third transistor, and the sixth transistor are each a P-type transistor.
4. (Original) A clocked inverter according to claim 1, wherein the third transistor is replaced with an analog switch.
5. (Canceled)
6. (Currently Amended) A clocked inverter according to claim 5, wherein:  
comprising:  
first to third transistors connected in series, and  
a fourth transistor and a fifth transistor connected in series, wherein:  
gates of the fourth transistor and the fifth transistor are connected to each other;

drains of the fourth transistor and the fifth transistor are each connected to a gate of the first transistor;

sources of the first transistor and the fifth transistor are each electrically connected to a first power source;

a source of the third transistor is electrically connected to a second power source;

an amplitude of a signal inputted to a source of the fourth transistor is smaller than a potential difference between the first power source and the second power source;

the first power source is a high potential power source;

the second power source is a low potential power source;

the first transistor and the fifth transistor are each a P-type transistor; and

the second to fourth transistors are each an N-type transistor.

7. (Currently Amended) A clocked inverter according to claim 5, wherein:  
comprising:

first to third transistors connected in series, and

a fourth transistor and a fifth transistor connected in series, wherein:

gates of the fourth transistor and the fifth transistor are connected to each other;

drains of the fourth transistor and the fifth transistor are each connected to a gate of the first transistor;

sources of the first transistor and the fifth transistor are each electrically connected to a first power source;

a source of the third transistor is electrically connected to a second power source;

an amplitude of a signal inputted to a source of the fourth transistor is smaller than a potential difference between the first power source and the second power source;

the first power source is a high potential power source;  
the second power source is a low potential power source;  
the first transistor, the second transistor, and the fifth transistor are each a P-type transistor; and  
the third transistor and the fourth transistor are each an N-type transistor.

8. (Currently Amended) A clocked inverter according to claim 5, wherein:  
comprising:

first to third transistors connected in series, and  
a fourth transistor and a fifth transistor connected in series, wherein:  
gates of the fourth transistor and the fifth transistor are connected to each other;  
drains of the fourth transistor and the fifth transistor are each connected to a gate  
of the first transistor;  
sources of the first transistor and the fifth transistor are each electrically  
connected to a first power source;  
a source of the third transistor is electrically connected to a second power  
source;  
an amplitude of a signal inputted to a source of the fourth transistor is smaller  
than a potential difference between the first power source and the second power  
source;  
the first power source is a low potential power source;  
the second power source is a high potential power source;  
the first transistor and the fifth transistor are each an N-type transistor; and  
the second to fourth transistors are each a P-type transistor.

9. (Currently Amended) A clocked inverter according to claim 5, wherein:  
comprising:

first to third transistors connected in series, and

a fourth transistor and a fifth transistor connected in series, wherein:  
gates of the fourth transistor and the fifth transistor are connected to each other;  
drains of the fourth transistor and the fifth transistor are each connected to a gate  
of the first transistor;

sources of the first transistor and the fifth transistor are each electrically  
connected to a first power source;

a source of the third transistor is electrically connected to a second power  
source;

an amplitude of a signal inputted to a source of the fourth transistor is smaller  
than a potential difference between the first power source and the second power  
source;

the first power source is a low potential power source;

the second power source is a high potential power source;

the first transistor, the second transistor, and the fifth transistor are each an N-type transistor; and

the third transistor and the fourth transistor are each a P-type transistor.

10. (Currently Amended) A clocked inverter according to claim [[5]] 6, wherein the fourth transistor is replaced with an analog switch.

11. (Currently Amended) A NAND comprising:

a first transistor and a second transistor ~~connected in series~~;

~~a third transistor connected to the first transistor and the second transistor in series;~~ and

a fourth transistor and a fifth transistor connected in series, wherein:

a drain of the first transistor is connected to a drain of the second transistor and a  
drain of the third transistor;

gates of the fourth transistor and the fifth transistor are connected to each other;

drains of the fourth transistor and the fifth transistor are each connected to a gate of the third transistor;

sources of the first transistor and the second transistor are each electrically connected to a first potential power source;

sources of the third transistor and the fifth transistor are each electrically connected to a second potential power source; and

an amplitude of a signal inputted to a source of the fourth transistor and each of gates of the first transistor, the second transistor, the fourth transistor, and the fifth transistor is smaller than a potential difference between the first potential power source and the second potential power source.

12. (Previously Presented) A NAND according to claim 11, wherein:

the first power source is a high potential power source;

the second power source is a low potential power source; and

the first transistor, the second transistor, and the fourth transistor are each a P-type transistor, and the third transistor and the fifth transistor are each an N-type transistor.

13. (Original) A NAND according to claim 11, wherein the fourth transistor is replaced with an analog switch.

14. (Currently Amended) A NOR comprising:

a first transistor and a second transistor ~~connected in series~~;

~~a third transistor connected to the first transistor and the second transistor in series; and~~

a fourth transistor and a fifth transistor connected in series, wherein:

a drain of the first transistor is connected to a drain of the second transistor and a drain of the third transistor;

gates of the fourth transistor and the fifth transistor are connected to each other; drains of the fourth transistor and the fifth transistor are each connected to a gate of the third transistor;

sources of the first transistor and the second transistor are each electrically connected to a first potential power source;

sources of the third transistor and the fifth transistor are each electrically connected to a second potential power source; and

an amplitude of a signal inputted to each of gates of the first transistor, the second transistor, the fourth transistor, and the fifth transistor and to a source of the fourth transistor is smaller than a potential difference between the first potential power source and the second potential power source.

15. (Previously Presented) A NOR according to claim 14, wherein:

the first power source is a low potential power source;

the second power source is a high potential power source; and

the first transistor, the second transistor, and the fourth transistor are each an N-type transistor, and the third transistor and the fifth transistor are each a P-type transistor.

16. (Original) A NOR according to claim 14, wherein: the fourth transistor is replaced with an analog switch.

17. (Previously Presented) A shift register comprising:

a clocked inverter including a first transistor to a third transistor connected in series; and

a fourth transistor and a fifth transistor connected in series, wherein:

sources of the first transistor and the fifth transistor are each electrically connected to a first power source;

a source of the third transistor is electrically connected to a second power source;

a gate of the first transistor is connected to drains of the fourth transistor and the fifth transistor;

a pulse generated at an (n-1)th stage is inputted to gates of the fourth transistor and the fifth transistor arranged at an n-th stage; and

a pulse or a clock signal generated at an (n-2)th stage is inputted to a source of the fourth transistor arranged at the n-th stage.

18. (Original) A shift register according to claim 17, wherein:

the first power source is a low potential power source;

the second power source is a high potential power source;

the first transistor and the fifth transistor are each an N-type transistor; and

the second to fourth transistors are each a P-type transistor.

19. (Original) A shift register according to claim 17, wherein:

the first power source is a high potential power source;

the second power source is a low potential power source;

the first transistor and the fifth transistor are each a P-type transistor; and

the second to fourth transistors are each an N-type transistor.

20. (Original) A shift register according to claim 17, wherein the fourth transistor is replaced with an analog switch.

21. (Original) A shift register according to claim 17, wherein the second transistor is eliminated.

22. (Previously Presented) A shift register comprising:

a plurality of stages each of which includes: a clocked inverter including a first transistor and a second transistor connected in series; an inverter; and a third transistor and an analog switch, wherein:

the first transistor is a P-type transistor,

the second transistor and the third transistor are each an N-type transistor;

a gate of the first transistor is connected to an output terminal of the inverter and a source of the first transistor is electrically connected to a high potential power source;

a gate of the second transistor is connected to a clock signal line through the analog switch and a source of the second transistor is connected to a low potential power source; and

the analog switch is connected to the output terminal of the inverter and an input terminal of the inverter.

23. (Previously Presented) A shift register comprising:

a plurality of stages each of which includes: a clocked inverter including a first transistor and a second transistor connected in series; an inverter; and a third transistor and an analog switch, wherein:

the first transistor is an N-type transistor,

the second transistor and the third transistor are each a P-type transistor;

a gate of the first transistor is connected to an output terminal of the inverter and a source of the first transistor is electrically connected to a low potential power source;

a gate of the second transistor is connected to a clock signal line through the analog switch and a source of the second transistor is connected to a high potential power source; and

the analog switch is connected to the output terminal of the inverter and an input terminal of the inverter.

24. (Previously Presented) A clocked inverter comprising:

a first transistor and a second transistor connected in series,  
a third transistor and a fourth transistor connected in series, and  
a fifth transistor and a sixth transistor connected in series, wherein:  
gates of the third transistor and the fourth transistor are connected to each other,  
drains of the third transistor and the fourth transistor are each connected to a  
gate of the first transistor,

sources of the first transistor and the fourth transistor are each electrically  
connected to a first power source,

sources of the second transistor and the sixth transistor are electrically  
connected to a second power source,

gates of the fifth transistor and the sixth transistor are connected to each other,  
drains of the fifth transistor and the sixth transistor are each connected to a gate  
of the second transistor,

a first signal is inputted to a source of the third transistor, and  
a second signal is inputted to a source of the fifth transistor.

25. (Previously Presented) A shift register comprising:

a first circuit inputted with a first signal;  
a second circuit inputted with a second signal;

a first clocked inverter electrically connected with the first and second circuits;

a third circuit comprising a first analog switch, inputted with the first signal;

a fourth circuit comprising a second analog switch, inputted with the second  
signal; and

a second clocked inverter electrically connected with the third and fourth circuits.

26. (Previously Presented) A clocked inverter according to claim 1, wherein the  
fifth transistor is replaced with an analog switch.

27. (Previously Presented) A shift register according to claim 17, wherein:  
the first power source is a low potential power source;  
the second power source is a high potential power source;  
the first transistor, the second transistor, and the fifth transistor are each an N-type transistor; and  
the third transistor and the fourth transistor are each a P-type transistor.
28. (Previously Presented) A shift register according to claim 17, wherein:  
the first power source is a high potential power source;  
the second power source is a low potential power source;  
the first transistor, the second transistor, and the fifth transistor are each a P-type transistor; and  
the third transistor and the fourth transistor are each an N-type transistor.
29. (Previously Presented) A shift register according to claim 22, wherein:  
a gate of the third transistor is connected to the input terminal of the inverter,  
a source of the third transistor is connected to the low potential power source,  
and  
a drain of the third transistor is connected to the gate of the second transistor.
30. (Previously Presented) A shift register according to claim 23, wherein:  
a gate of the third transistor is connected to the input terminal of the inverter,  
a source of the third transistor is connected to the high potential power source,  
and  
a drain of the third transistor is connected to the gate of the second transistor.
31. (Previously Presented) A shift register according to claim 25, wherein:

the first clocked inverter comprises a first transistor and a second transistor in series,

the first circuit comprises a third transistor and a fourth transistor in series,

the second circuit comprises a fifth transistor and a sixth transistor in series, and

the second clocked inverter comprises a seventh transistor and an eighth transistor in series.

32. (Previously Presented) A shift register according to claim 25, further comprising an inverter.

33. (New) A clocked inverter according to claim 7, wherein the fourth transistor is replaced with an analog switch.

34. (New) A clocked inverter according to claim 8, wherein the fourth transistor is replaced with an analog switch.

35. (New) A clocked inverter according to claim 9, wherein the fourth transistor is replaced with an analog switch.